REMARKS

The Examiner's indication of allowability of claims 7 and 8, if rewritten in independent form, is acknowledged and appreciated.

Claims 5 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki et al. in view of Takehashi et al. Applicants respectfully traverse this rejection because the cited references, even if combined, still would not disclose or suggest at least the second gate insulation film being formed on the first gate insulation film, and an insulation film that is formed on the second gate electrode and is of the same material as the second gate insulation film. The cited references also do not disclose or suggest both the first and second gate insulation films being formed on or over the semiconductor layer.

As shown in Fig. 16, Yamazaki discloses two thin film transistors having a first gate insulation film 805, active layers 806 and 807 formed on the first gate insulation 805, and second and second gate insulation films 808 and 809 formed on the active layers 806 and 807. Gate electrodes 813 and 814 are formed on the second gate insulation films 808 and 809. Yamazaki, however, fails to disclose a second gate insulation film 26 being formed on the first gate insulation film 24, and an insulation film that is formed on the second gate electrode 25a (or 25b) and is formed of the same material of which the second gate insulation film 26 is formed (see Fig. 5C, for example).

Furthermore, claim 5 calls for both the first and second gate insulation films 24, 26 being formed on or over the semiconductor layer. The structure of Yamazaki, in contrast, discloses that the first gate insulation film 805 is formed under the active layers (the semiconductor layers) 806 and 807, and that the second insulation films 808 and 809 are formed on the active layers 806 and 807.

Moreover claim 5 recites that, the first gate electrode 271 is formed in the first thin film transistor, and the second gate electrode 25a is formed in the second thin film transistor. On the other hand, in the structure of Yamazaki, each thin film transistor has two gate electrodes, the gate electrode 813 (814) formed on the active layer 806 (807) and the back gate electrode 803 (804) formed under the active layer 806 (807).

Takehashi is mere cited for disclosing a semiconductor layer having lightly doped source/drain regions. This reference also fails to disclose or suggest at least the features of the invention described above. Therefore, even if the references were combined, they still would not disclose or suggest the subject matter of claim 5. Accordingly, claim 5 and its dependent claim 6-8 are allowable over the cited references.

For all of the above reasons, Applicants request reconsideration and allowance of the claimed invention. The Examiner should contact Applicants' undersigned attorney if a telephone conference would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

B. Joe Kim
Registration No. 41,895

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Suite 2500
300 South Wacker Drive
Chicago, Illinois 60606
(312) 360-0080
Customer No. 24978
P:\DOCS\1324\68134\726562.DOC